Stacked DRAM: The Hybrid Memory Cube

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A look ahead through Nvidia's GPU roadmap
A 2013 graphics card: Kepler GPU with GDDR5 video memory
A 2017 graphics card: Volta GPU with Stacked DRAM
# A promising Stacked DRAM development: The Hybrid Memory Cube Consortium (HMCC)

<table>
<thead>
<tr>
<th>HMCC achievements and milestones</th>
<th>Date</th>
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<tbody>
<tr>
<td>First papers published about Stacked DRAM (based of research projects)</td>
<td>2005, 2006</td>
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<td>First commercial announcement of the technology</td>
<td>February, 2011</td>
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<td>HMC Consortium is launched by Micron Technologies and Samsung Electronics</td>
<td>October, 2011</td>
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<td>Stacked DRAM announced for Volta GPU by Nvidia</td>
<td>March, 2013</td>
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<tr>
<td>Specification 1.0 available</td>
<td>April, 2013</td>
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<tr>
<td>Production samples</td>
<td>Second half of 2014 (estimated)</td>
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<tr>
<td>2.5 configuration available</td>
<td>End of 2014 (estimated)</td>
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</table>
Developer members of HMCC (as of May'13)

- Altera Corporation
- ARM
- IBM
- Micron Technology, Inc
- Open-Silicon, Inc.
- Samsung Electronics Co., Ltd
- SK hynix
- Xilinx, Inc.

Founders of the consortium
HMC was primarily oriented to HPC and networking, but it can also be useful for mobile and DDR-like technol.

HMC is tightly coupled with CPUs, GPUs and ASICS in point-to-point configurations, where HMC performance is available for optical memory bandwidth.
The Hybrid Memory Cube at a glance

Revolutionary Approach to Break Through the “Memory Wall”

► Evolutionary DRAM roadmaps hit limitations of bandwidth and power efficiency
► Micron introduces a new class of memory: Hybrid Memory Cube
► Unique combination of DRAMs on Logic

Key Features

► Micron-designed logic controller
► High speed link to CPU
► Massively parallel “Through Silicon Via” connection to DRAM

Unparalleled performance

► Up to 15X the bandwidth of a DDR3 module
► 70% less energy usage per bit than existing technologies
► Occupying nearly 90% less space than today’s RDIMMs

Full silicon prototypes in silicon TODAY

Targeting high performance computing and networking, eventually migrating into computing and consumer
Architectural highlights

- Stacked DRAM is an abstracted memory management layer.
- The traditional DRAM core cell architecture is restructured to use memory vaults rather than arrays.
- A logic controller is placed at the base of the DRAM stack.
- The assembly is interconnected with through-silicon vias (TSVs) that go up and down the stack.
- The final step is advanced package assembly.
Architectural details

1. DRAM is partitioned into 16 parts like DDR3 and DDR4.
2. Common logic is extracted from all partitions.
3. DRAM is piled up in 4-high or 8-high configurations.
4. Common logic is re-inserted at the logic base die.
5. 16 vaults are built. Each consists of either 4 or 8 parts of each layer plus logic underneath, and can be thought of as individual channels in the regular architecture.
6. A high speed link connects DRAM and processor, with:
   1. Advanced switching.
   2. Optimized memory control.
   4. 16 transmits and receive lanes, each running at 10 GB/s.
Add advanced switching, optimized memory control and simple interface to host processor(s)…
HMC supports stacked DRAM in two different flavours: Near memory and far memory.
HMC near memory

- All links between CPU and HMC logic layer.
- Maximum bandwidth per GB. capacity.

Target systems:
- HPC and servers.
- Hybrid CPU/GPU platforms.
- Graphics.
- Networking.
- Test equipment.
HMC far memory

- Far memory
  - Some HMC links connect to host, some to other cubes.
  - Scalable to meet system requirements.
  - Can be in module form or soldered-down.

- Future interfaces may include
  - Higher speed electrical (SERDES)
  - Optical
  - Whatever the best interface for the job!
A comparison in bandwidth with existing technologies

On a CPU system (PC with a dual channel motherboard):

- [2013] DDR3 @ 4 GHz (2x 2000 MHz): 64 Gbytes/s.
- [2015] HMC 2.0 (second generation): **898 Gbytes/s**.

A 2x improvement can be reached in a quad-channel motherboard.

On a GPU system (384-bits wide graphics card):

- GDDR5 @ 7 GHz: 336 Gbytes/s.

12 chips 32-bits wide are soldered to the printed circuit board, where HMC 2.0 chips achieve **2688 Gbytes/s** (2.62 Tbytes/s).
Additional information available on the Web

The Hybrid Memory Cube Consortium:
http://www.hybridmemorycube.org (specification 1.0 available as PDF).

CUDA Education (presentations, exercises, tools, utilities):

Keynotes and technical sessions from GTC'13:
You will find more than 300 talks. Particularly recommended:

"Future directions for CUDA" by Mark Harris.
"Multi-GPU Programming" by Levi Barnes.
"Performance Optimization Programming Guidelines..." by Paulius Micikevicius.
"Performance Optimization Strategies for GPU-accel. Applications" by David Goodwin.
"Languages, Libraries and Development Tools for GPU Computing" by Will Ramey.
"Getting Started with OpenACC" by Jeff Larkin.
"Optimizing OpenACC Codes" by Peter Messmer.
Acknowledgements

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- Stephen Jones [2012: Kepler].
- David B. Kirk [2008-2009: Nvidia hardware].
- David Luebke [2007-2008: Nvidia hardware].
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... just to name a few of those who contributed to my presentations.

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